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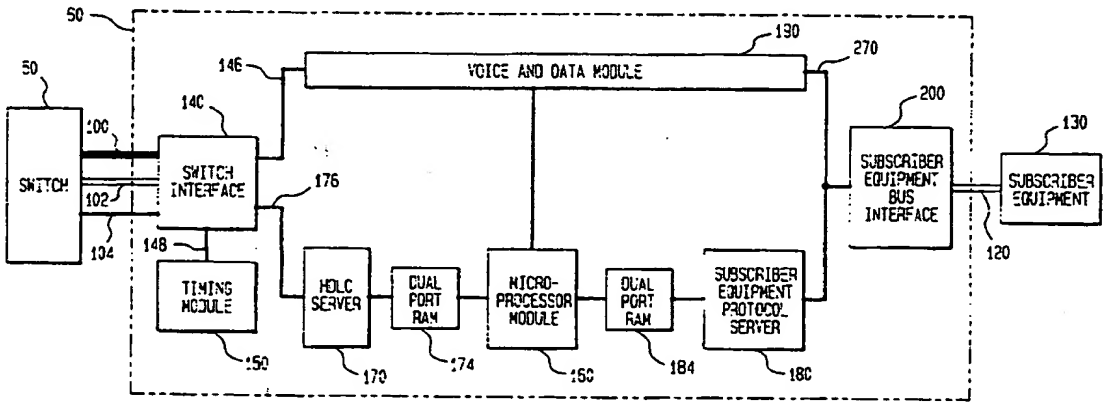

(57) Abstract

An interfacing device can be used to interconnect telephone systems otherwise incompatible because of differences in data, control, and timing formats and protocols. The interfacing device provides a transparent link, performing all of the necessary conversions to enable seamless bidirectional communication.

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Telecommunications System Interfacing Device and Method

Field of the Invention

This invention generally relates to telecommunications systems. Specifically, the invention concerns a device that allows one to interconnect two telecommunications systems that are otherwise incompatible due to differences in data and signalling formats.

Background of the Invention

Until perhaps fifteen years ago, telephone technology for business applications was limited in capability and features. Most equipment was of the "key set" variety, permitting access to a set number of lines from individual desktop units. Since then, and largely with the advent of computer technology and LSI (large-scale integration), the industry has produced a wide array of digital telephone systems with a great number of options.

To this day, the technology is changing so rapidly that it would be impractical for a business to keep up with the latest innovations. For example, one might have a significant investment in desktop devices and associated peripherals and cabling, but wishes to take advantage of the benefits of a new switch. If this new switch uses a set of formats and protocols incompatible with the subscriber equipment, this would require the purchase and installation of a completely new telephone system. Such an option is costly and therefore generally not practical.

Thus, an interface between one portion of a telecommunications system, such as a switch, using one set of formats and protocols and another portion, such as subscriber devices, using a different set of formats and protocols, would be very useful. Additionally, such a device would be helpful in interconnecting other types of telephone communications equipment with differing

protocols, even entire self-standing systems such as PABXs (private automatic branch exchanges).

Throughout this description, it should be understood the term "data" represents, where appropriate, both data and voice signals. The term "control" represents, where appropriate, both control and status report signals.

Summary of the Invention

This and other objects are achieved by the interfacing device described here. The device accepts data, control, and timing information in one set of formats and translates that information into another set of formats. In one embodiment, in the context of a PABX, one set of such information is compatible with a switch and another set is compatible with subscriber equipment. The first set consists of voice and data signals transmitted in timeslots on serial data highways, control information serially transmitted in a link layer format such as HDLC, and timing signals. The second set, compatible with the subscriber equipment, utilizes a different set of formats -- all information passes on a parallel-bus structure. Moreover, certain control information is time-division multiplexed with the voice and data.

The interfacing device has the task of taking data, control, and timing information from the switch and passing this to the subscriber equipment in an intelligible form. Similarly, in the reverse direction, the interfacing device will take data, control, and timing information from the subscriber equipment and pass these signals to the switch in a form recognized by the switch. To accomplish this, the device has several subsystems, including one interface that communicates with the switch and another interface that communicates with the subscriber equipment. A timing module, using the timing and synchronization output of the switch, generates the timing signals necessary to operate the interface device. The timing of the subscriber

equipment is arbitrarily slaved to the timing of the switch.

The conversion of the formats of the voice and data signals takes place in a voice and data module. Because voice and data signals can flow in either direction, the process is bidirectional.

A similar conversion must occur for control signals. The device has a subsystem that takes the control signals from one telecommunications system and converts them to a format compatible with the other system. Again, this is a bidirectional process. In one embodiment of the invention, this function is distributed across three units, one handling control signals from one side, another handling control signals from the other side, and a third performing the actual conversion.

Brief Description of the Drawings

A more complete understanding of the present invention, as well as other objects and advantages thereof not enumerated herein, will become apparent upon consideration of the following detailed description and the accompanying drawings, wherein:

Figures 1 and 2 are schematic block diagrams of telecommunications systems;

Figure 3 is a schematic block diagram of the interfacing device;

Figure 4 is a schematic block diagram of the switch interface;

Figure 5 is a schematic block diagram of the timing module;

Figure 6 is a schematic block diagram of the microprocessor module;

Figure 7 is a schematic block diagram of the HDLC server;

Figure 8 is a schematic block diagram of the subscriber equipment protocol server;

Figure 9 is a schematic block diagram of the voice and data module;

Figure 10 is a schematic block diagram of the subscriber equipment bus interface;

Figure 11 is a diagram illustrating the voice/data and control formats of the switch and the subscriber equipment; and

Figure 12 is a timing diagram of the signals on the subscriber equipment bus.

Detailed Description of the Invention

The general case of the interfacing device interconnects two or more telecommunications systems or, as will be discussed here, two portions of one telecommunications system, where each utilizes unique formats and protocols.

Consider first the case of a telecommunications system having fully compatible components. As illustrated in Figure 1, the telecommunications system 10 has a switch 12 communicating through a conduit 14 with an expander 20 or another similar device. The expander 20 in turn is connected by connectors 22 to a series of line cards 30, each of which is connected by a line 32 to at least one and probably several terminal devices 40. The system 10 functions in part because the formats of the data, signalling, and timing information are intelligible to all of the components.

Should one substitute a switch having an entirely different format in the system of Figure 1, it would fail. However, such a substitution may be accomplished as illustrated in the telecommunications system 42 shown in Figure 2. A new switch 50, although utilizing incompatible formats and protocols, is connected by conduit 52 to an intermediary interfacing device 60 that bridges the differences between the switch and the subscriber equipment, and replaces the expander 20. In the following discussion, it should be understood that the respective

formats of either side are arbitrary; different formats could have been employed.

A. The Formats and Protocols of the Switch

In the system of Figure 2, the switch 50 passes data, control, and timing information on a conduit 52 that in actuality includes several separate paths. Referring to Figure 3, data and voice pass between the switch 50 and the interfacing device 60 on serial data highways 100. Control information, in this case in an HDLC format, passes between the switch 50 and the interfacing device 60 on a serial HDLC link 102. Timing and synchronization information is transferred from the switch 50 to the interfacing device 60 over timing and synchronization lines 104.

To obtain the desired throughput, the switch 50 connects to eight serial data highways 100. Four of the highways 100 carry incoming traffic; the other four highways 100 carry outgoing traffic. Incoming refers to traffic flowing from the switch to the subscriber equipment; outgoing is the reverse direction. Using time-division multiplexing, each highway 100 is arbitrarily time-divided into 64 channels or timeslots, each containing 8 bits, collectively providing a total of 256 incoming and 256 outgoing channels. The channels may carry voice, data (64 kbps synchronous or asynchronous up to 19.2 kbps), or any combination of these. Every connection to a terminal device occupies an incoming timeslot and an outgoing timeslot. Further, data and voice are encoded using pulse code modulation (PCM). As is standard among some telephone systems, the repetition rate of the timeslots is 8000 times per second resulting in a period of 125 microseconds and a bit rate on each highway 100 of 4.096 Mbps. On each serial highway, each group of 64 channels or timeslots constitutes a frame. Within the interfacing device 60, a frame consists of 256 incoming channels and 256 outgoing channels.

No control information is passed on the serial data highways 100 nor are there any framing bits, headers,

flags, or other delimiters. Although such headers and flags may occur within a given channel, they only have meaning to the terminal equipment and are not recognized by the interfacing device 60.

The HDLC link 102 operates at a bit rate of 2.048 Mbps and the timing and synchronization lines 104 provide a 2.048 MHz clock signal and a 4 kHz frame synchronization pulse. The frame synchronization pulse is used by the interfacing device to determine the beginning of the timeslot frames on the serial data highways 100.

B. The Formats and Protocols of the Subscriber Equipment

Subscriber equipment 130 (e.g., the line cards 30 and associated terminal devices 40 of Figure 2) communicates with the switch 50 through a connector 22 (Figure 2). In the embodiment under discussion, the connector 22 is shown in Figure 3 as a subscriber equipment bus 120. The subscriber equipment bus 120 is a time-division multiplexed parallel-format bus carrying data (including voice), addressing, control information, and clock timing. The bus has four components: a data segment 310, an address segment 312, a line card enable segment 314, and a timing segment 316 (see Figure 10).

The data segment 310 is distributed across 16 lines and transfers data and control information in frames of 576 timeslots that repeat every 125 microseconds, or 8000 times per second. The bit rate on each line of the data segment 310 is therefore 4.608 Mbps.

Each frame of the data segment 310 is arbitrarily divided into two parts: an immediate field and a permanent field (see the subscriber equipment bus 120 in the timing diagram in Figure 11). The immediate field has 64 timeslots that convey control information. The permanent field has 512 timeslots in which voice and data are carried.

The address segment 312 provides the line card with the identity of the terminal device 40 assigned to a given

timeslot while the line card enable segment 314 selects the proper line card 30. Finally, the timing segment 316 contains the timing signals required for synchronizing the subscriber equipment 130 with the switch 50 and the interfacing device 60. Although bundled together with the data, address, and line card enable segments 310, 312, and 314, the timing segment 316 is not time-division multiplexed but rather a free-running 4.608 MHz clock line and an 8 kHz frame synchronization line.

Again, the reader should recognize that the stated formats of the serial data highways 100, the HDLC link 102, the timing and synchronization lines 104, and the subscriber equipment bus 120 are arbitrary as far as the interfacing device 60 is concerned. The particular formats and protocols are dictated by the respective formats and protocols of the switch 50 and the subscriber equipment 130 and either or both of these could well have utilized different formats and protocols.

C. Interfacing Device Requirements

In order to connect the switch 50 to the subscriber equipment 130, each of which communicates using the formats described above, the data, control, and timing information must be converted from one set of formats to the other and back again. To function without hindering the passage of telephone calls, the interfacing device 60 must be transparent to the user. Moreover, looking from the perspective of the switch 50, the interfacing device 60 must emulate compatible interconnecting devices using the same formats and protocols, i.e., the serial data highways 100, the HDLC link 102, and the timing and synchronization lines 104. Similarly, from the perspective of the subscriber equipment 130, the interfacing device 60 must emulate the expander 20 of Figure 1. In addition to reformatting voice and data traffic, the interfacing device 60 must reformat the HDLC control protocol of the switch 50 to the control protocol of the subscriber equipment bus 120

and vice versa. The respective formats of the two systems are contrasted in Figure 11.

D. The Structure and Operation of the Interfacing Device

As shown in Figure 3, the interfacing device 60 contains several subsystems. These include a switch interface 140, a timing module 150, a microprocessor module 160, an HDLC server 170, a subscriber equipment protocol server 180, a voice and data module 190, and a subscriber equipment bus interface 200. Each of these are dealt with individually below.

Although a single, sufficiently powerful microprocessor could be employed to handle all computing functions in the interfacing device 60, the processing in the embodiment of Figure 3 is distributed over three separate, general purpose 80186/88 microprocessors. A main microprocessor 162 resides in the microprocessor module 160 (see Figure 6), an HDLC microprocessor 172 resides in the HDLC server 170 (see Figure 7), and a subscriber equipment protocol microprocessor 182 is located in the subscriber equipment protocol server 180 (see Figure 8). Adjacent processors communicate through respective HDLC and protocol server dual port RAMs 174 and 184.

In addition to the microprocessors, the interfacing device 60 uses field programmable gate arrays ("FPGAs"). These can be configured by the user to provide logic functions. In the embodiment under discussion, Xilinx 3000 FPGAs, available from Xilinx, 2100 Logic Drive, San Jose, California, were used. These components, as well as the methods for configuring and programming them, are described in detail in the 1992 Xilinx Programmable Gate Array Databook.

For purposes of simplifying the presentation, address bussing for the components of the interfacing device 60 is not shown in the drawings except where necessary to explain the structure or operation of the device. Additionally,

both volatile and non-volatile memory are shown simply as RAM in Figures 6, 7, and 8.

1. The Switch Interface

Within the interfacing device 60, the serial data highways 100, the HDLC link 102, and the timing and synchronization lines 104 are connected to a switch interface 140, as shown in Figure 4. The switch interface 140 distributes data, HDLC, and timing signals to the other components of the interfacing device 60. Also, the switch interface 140 provides the conversion between the serial bit format used on the serial data highways 100 and the parallel format used internally by the interfacing device 60. A serial-to parallel/parallel-to-serial converter 142 implemented in a single FPGA 144 performs the conversion. Alternatively, this function could be split among separate serial-to parallel and parallel-to-serial converters.

The switch interface 140 has three outputs. A data output 146 connects switch interface 60 with the voice and data module 190. An internal HDLC link 176 carries the HDLC controls signals between the switch interface 140 and the HDLC server 170. Finally, a timing output on lines 148 provides the 2.048 MHz clock signal and the 4 kHz frame synchronization pulse to the timing module.

2. Timing Module

As shown in Figure 5, the timing module 150 receives the 2.048 MHz clock signal and the 4 kHz frame synchronization pulse on timing and synchronization lines 148. Internally, lines 148 split into a timing line 206, carrying the 2.048 MHz clock signal, and a synchronization line 208, carrying the 4 kHz frame synchronization pulse.

The 2.048 MHz clock signal is supplied to a phase-locked loop 210 to generate a 36.864 MHz output signal 212. This signal is supplied to a timing module 214, which can be implemented in an FPGA configured to perform a divide-by-two function, to generate an 18.432 MHz system clock signal 216. As will be explained below, the

interfacing device 60 uses the system clock signal 216 to generate a timing signal for the subscriber equipment bus 120. Although not shown, the timing module 150 uses the frame synchronization pulse 208 to determine the start of frames on the serial data highways 100.

3. Microprocessor Module

The microprocessor module 160, containing the main microprocessor 162, essentially controls the interfacing device 60, acting in response to signals received from the switch 50 and the subscriber equipment 130. As shown in Figure 6, the microprocessor module 160 has a microprocessor RAM 164 for storing software functions and any control signals that need to be processed. A common bus 166 runs throughout the module 160, interconnecting the main microprocessor 162 and the RAM 164, as well as connecting the microprocessor to other subsystems of the interfacing device 60.

The microprocessor module 160 is charged with running a connection manager and a control signal converter. Both of these are resident software functions stored in the microprocessor RAM 164. Essentially a scratchpad, the connection manager sets up and tears down connections. The control signal converter performs the conversion of control signals from the HDLC format to the subscriber equipment format and back again.

The control signal converter uses a combination of state machines and look-up tables. State machines are adaptive, dynamic software modules that may produce a response, depending upon the input. By contrast, look-up tables are fixed, static devices that have a one-to-one relationship between their inputs and outputs. For example, upon receipt of an HDLC signal from the switch 50, the main microprocessor 162 will determine what response is required, if any, to meet the control protocol of the subscriber equipment 130. Similarly, upon receipt of a control signal from the subscriber equipment 130, the main microprocessor 162 will ascertain what response is

required, if any, to meet the control protocol of the switch 50. State machines are discussed in greater detail in the text The Art of Electronics, by Paul Horowitz and Winfield Hill (Cambridge University Press, 2nd Edition, 1990), pp. 512-38.

4. HDLC Server

The HDLC server 170 provides an interface between the HDLC link 102 of the switch 50 and the main microprocessor 162, acting largely as a buffer. HDLC messages originating at the switch 50 pass along the HDLC link 102, through the switch interface 140, and then onto the internal HDLC link 176 where they are picked up by the HDLC server 170. Similarly, HDLC messages sent by the main microprocessor 162 for transmission to the switch 50 are read by the HDLC server 170 from the HDLC dual port RAM 174 and are ultimately placed on the internal HDLC link 176, passed through the switch interface 140, and then placed on the HDLC link 102.

Internally, as illustrated in Figure 7, the HDLC server 170 has an HDLC engine 280, an HDLC controller 282, an HDLC microprocessor 172, and an HDLC RAM 284. The latter three components are interconnected by an HDLC server bus 288. The HDLC engine acts as a bidirectional transceiver and can be implemented in an FPGA. The HDLC controller can be a Siemens SAB 82525 High-Level Serial Communications Controller Extended (HSCX).

An HDLC message from the switch 50 is initially received in the HDLC server 170 on the internal HDLC link 176 by the HDLC engine 280. The HDLC engine 280 checks the message to determine if it contains an information frame (one type of frame within the HDLC format) for an address within a previously-defined range. If so, the engine 280 passes the message on line 286 to the HDLC controller 282, which checks for message integrity, using a method such as cyclic redundancy checking. The message is then passed on bus 288 to the HDLC dual port RAM 174 where it is accessed by the HDLC microprocessor 172. The microprocessor 172

converts the message to a stripped-down HDLC format compatible with the main microprocessor 162. The converted message remains in the HDLC dual port RAM 174 until retrieved by the main microprocessor 162.

If the message originates in the subscriber equipment 130, it is passed by the main microprocessor 162 to the HDLC server 170 through the HDLC dual port RAM 174. The message passes on bus 288 to the HDLC RAM 284 where it is held until converted into the proper format for the HDLC link 102 by the HDLC microprocessor 172. The HDLC engine 280 then receives the reformatted message from the HDLC controller 282 and places it on the internal HDLC link 176 for transmission back to the switch 50.

5. Subscriber Equipment Protocol Server

The subscriber equipment protocol server 180, shown in detail in Figure 8, handles the control functions specific to the subscriber equipment, and serves as an interface between the subscriber equipment bus 120 and the main microprocessor 162. In addition to its microprocessor 182, the subscriber equipment protocol server 180 has a protocol server engine 290, which can be implemented in an FPGA, overseeing the flow of control signals between the subscriber equipment bus 120 and the microprocessor module 160. It also has a protocol server RAM 292 that holds control information in the protocol server 180 until accessed by either the server engine 290 or the microprocessor 182.

The protocol microprocessor 182, the protocol server dual port RAM 184, the protocol server RAM 292, and the protocol server engine 290 are interconnected by a protocol server bus 294. The protocol server engine 290 is also connected by the internal data bus 270 to the subscriber equipment bus interface 200.

Control information passing from the switch 50 to the subscriber equipment 130 is handled in the following manner. During the permanent field interval, the protocol microprocessor 182 reads control signals from the protocol

server dual port RAM 184 and writes them into the server RAM 292. During the immediate field interval, the protocol server engine 290 takes the control information for the subscriber equipment bus from the protocol server RAM 292, including addressing information specifying a line card destination, and places it on the internal data bus 270 for the subscriber equipment bus interface 200.

When passing control information originating at the subscriber equipment 130, the protocol server engine 290 receives information from the subscriber equipment bus interface 200 during the immediate field interval and writes it into the protocol server RAM 292. The protocol microprocessor 182 then takes the information in the protocol server RAM 292 and passes it to the protocol server dual port RAM 184, for eventual access by the main microprocessor 162.

6. Voice and Data Module

To convert the voice and data from the format of the switch 50 to the format of the subscriber equipment 130, the 512 PCM highway timeslots on the eight serial data highways 100 from the switch 50 are mapped on a one-to-one basis into the 512 permanent field timeslots on the subscriber equipment bus 120, yielding 256 simultaneous bidirectional connections. As shown in Figure 9, the mapping is performed in the voice and data module 190 by uplink and downlink voice/data processors 230 and 232, respectively, which can be implemented in FPGAs. The term uplink refers to the flow of data from the subscriber equipment 130 to the switch 50 while downlink refers to the flow from the switch 50 to the subscriber equipment 130.

Internally, the voice/data processors 230 and 232 are hard-wired to carry out the mapping between the two formats. The processors 230 and 232 are connected to the switch interface 140 by line 146 and to the subscriber equipment bus interface 200 by the internal data bus 270.

MAPPING			
Serial Highway Uplink Timeslot	Subcriber Interface Bus Uplink Timeslot	Serial Highway Downlink Timeslot	Subscriber Interface Bus Downlink
0	C_0	0	C_1
1	C_2	1	C_3
2	C_4	2	C_5
•	•	•	•
•	•	•	•
•	•	1	•
253	C_{506}	253	C_{507}
254	C_{508}	254	C_{509}
255	C_{510}	255	C_{511}

Table 1 - Mapping of Timeslots

The mapping relationship is illustrated logically in Table 1 above. The actual location of the timeslots in time may vary depending on time spacing requirements of the line cards. For example, in order to access more than one terminal device 40 on the same line card 30, one may need to use non-adjacent timeslots to provide sufficient time for the line card 30 to be enabled.

The data passing through the voice and data module 190 is cycled through uplink and downlink data buffers 234 and 236 connected to respective uplink and downlink voice/data processors 230 and 232 by lines 272 and 274, respectively. Although the data initially enters a voice/data processor 230 or 232, it is directly routed to a data buffer 234 or 236 for subsequent retrieval and processing by its respective voice/data processor 230 or 232.

Voice and synchronous data pass through the interfacing device 60 sequentially without being delayed

beyond one frame because of the direct one-to-one mapping relationship. However, asynchronous data calls are configured in a 128 kbps data format on the subscriber equipment bus 120, occupying 2 bytes per channel (8 data bits and 8 control bits), while the serial data highways 100 can only accommodate 8 bits per channel at 64 kbps. When there is a burst of asynchronous data passing from the subscriber equipment bus 120 to the switch 50, the data buffer 234 will accumulate a portion of the traffic in an 8-byte memory queue until the traffic can be passed on to the serial data highways 100. Nevertheless, the delay is negligible and in any event transparent to the user. Thus, the interfacing device 60 affords real-time transfer of voice and data.

The voice and data module 190 also contains a connection table 240. The connection table 240 stores the physical address of the particular item of subscriber equipment 130 utilizing a given timeslot for a call. The main microprocessor 162, using the connection manager software function, makes the necessary entries into the connection table 240 during the call setup process, and erases entries upon call completion. Although not shown in Figure 9, the voice and data module 190 could have gain adjustment provisions for adjusting the path gain and loss, independently in each direction, between the switch 50 and the subscriber equipment 130.

In lieu of separate data buses for passing voice/data and the timeslot designations in the connection table 240, the voice and data module 190 has a unified internal data bus 270 connected to the uplink and downlink voice/data processors 230 and 232, and the connection table 240. The processors 230 and 232 and the table 240 are accessed at separate times, maintaining the integrity of their respective data.

7. Subscriber Equipment Bus Interface

The subscriber equipment bus interface 200 provides the electrical and timing interface between the subscriber

equipment bus 120 and the interfacing device 60. It also provides the subscriber equipment 130 with the appearance of being connected to a now-replaced expander 20.

Timing for the subscriber equipment bus 120 is generated by a division function in a subscriber bus interface controller 300, as shown in Figure 10, which can be implemented in an FPGA. Dividing by four, the controller 300 generates a 4.608 MHz data clock on line 316 from the 18.432 MHz system clock signal 216 generated in the timing module 150. The 8 kHz frame synchronization signal, used by the subscriber equipment 130 to determine when each frame begins, is not shown separately but should be understood to be included in line 316.

The subscriber equipment bus interface 200 is connected to the subscriber equipment protocol server 180 and the voice and data module 190 by the internal data bus 270. The controller 300, in concert with a bidirectional line driver/transceiver 302 enabled by control lines 304, controls the flow of data. Similarly, the flow of addressing and control information from the interfacing device 60 to the subscriber equipment bus 120 is controlled by line drivers 306. The line drivers 306 are also enabled by control lines 304 as required.

The transmission of voice or data and control is split time-wise over the course of the 576 timeslots of the subscriber equipment bus 120 frame. During the 64 immediate field timeslots, the subscriber equipment bus interface 200 communicates with the subscriber equipment protocol server 180, transferring control information. During the 512 permanent field timeslots, the subscriber equipment bus interface 200 communicates with the voice and data module 190, transferring voice and/or data and the information contained in the connection table 240. One method of handling both is by interleaving the respective information.

The connection between the subscriber equipment bus interface 200 and the subscriber equipment bus 120 has four

elements: a bidirectional data segment 310, an address segment 312, a line card enable segment 314, and a timing segment 316. The timing relationship of the four segments is illustrated in Figure 12. The 8 kHz frame synchronization signal for the subscriber equipment 130 is not shown but again it should be understood that this signal is included in line 316.

Operation

The operation of the device will now be explained initially with reference to Figure 3. As can be seen, the interfacing device 60 handles essentially three types of signals: data, control, and timing. This is accomplished in two parallel paths -- the first being the voice and data module 190 for voice and data, and the second being the combination of the HDLC server 170, the microprocessor module 160, and the subscriber equipment protocol server 180 for the control signals. The paths are joined at one end by the switch interface 140 and at the other end by the subscriber equipment bus interface 200.

When a call for a subscriber equipment 130 terminal device 40 arrives through the switch 50, the switch 50 will send a control message to the terminal device 40 to set up a communications path. The control message, in HDLC format, is placed on the HDLC link 102, passes through the switch interface 140, onto the internal HDLC link 176, and into the HDLC server 170 and then into the HDLC dual port RAM 174.

Using the state machine and stored look-up table software functions, predetermined by the respective formats and protocols of the switch and the subscriber equipment employed by the user, the main microprocessor 162 converts the HDLC message to the control format of the subscriber equipment 130. For example, the first message from the switch 50 requests the initiation of a connection. The main microprocessor 162 in turn issues a seize command, which passes through the protocol server dual port RAM 184 to the subscriber equipment protocol server 180. During

the immediate field interval, the seize command message passes through the subscriber equipment bus interface 200 and onto the subscriber equipment bus 120.

Depending on the signalling protocols employed, the subscriber equipment 130 may at this point send a return message. To do so, the message is placed in the immediate field of the subscriber equipment bus 120, passed through the subscriber bus interface 200, and picked up by the subscriber equipment protocol server 180. The server 180 will pass the control message to the microprocessor module 160 for conversion to the HDLC format. The HDLC-formatted message now passes through the HDLC server 170, the switch interface 140 and onto the HDLC link 102 for access by the switch 50.

Ultimately, the switch 50 will select a timeslot for the communications path and convey it to the interfacing device 60 in an HDLC message placed on the HDLC link 102. The timeslot designation is written by the main microprocessor 162 into the connection table 240 and then conveyed to the subscriber equipment 130 on the address lines 312 of the subscriber equipment bus 120.

Once a voice/data path is selected, the switch 50 will permit passage of data. The voice or data will be placed in the selected timeslot on the serial data highways 100 and enter the switch interface 140 where it is converted from a serial format to a parallel format. The voice/data signal will then enter the voice and data module 190 where the downlink voice/data processor 232 will map the signal into the proper timeslot on the subscriber equipment bus 120. Then, during the permanent field interval, the subscriber equipment bus interface 200 will place the voice/data signal onto the subscriber equipment bus 120.

In the reverse direction, the terminal device sends its voice or data on the subscriber equipment bus 120, through the subscriber bus interface 200, and into the voice and data processor 190. The uplink voice/data processor 230 takes the voice or data and maps it into the

designated timeslot on the serial data highways 100. The voice or data is then reformatted from parallel to serial in the switch interface 140 and placed on the appropriate serial data highway 100 for reception by the switch 50.

If a call originates at the subscriber equipment 130, the terminal device 40 sends a control message back to the switch requesting a communications path. The switch 50 will then select a communications path for the terminal device 40, sending back the timeslot designation.

The actual mechanics of signalling are a matter of design choice and how the equipment at each end goes about polling for availability of terminal devices and lines, setting up and tearing down connections, and performing diagnostics will depend largely on the nature of the switch and the subscriber equipment employed. Therefore, because the resulting formats and protocols are likewise arbitrary and a matter of design choice, the details of the state machines and look-up tables that can be employed by the main microprocessor 162 have not been specified.

While there has been described what is believed to be the preferred embodiment of the invention, those skilled in the art will recognize that other and further modifications may be made thereto without departing from the spirit of the invention, and it is intended to claim all such embodiments that fall within the true scope of the invention.

What is claimed is:

1. An apparatus for interfacing at least two communications devices, each device accepting data and control signals, and each device having formats for data and control signals, comprising:

means for converting the format of the data from the format of one device to the format of another device; and

means for converting the format of the control signals from the format of one device to the format of another device.

2. An apparatus as set forth in claim 1, wherein the means for converting the format of the data includes means for converting the format in real time.

3. An apparatus as set forth in claim 1, wherein the means for converting the format of the control signals includes means for converting the format in real time.

4. An apparatus as set forth in claim 1, wherein the means for converting the format of the data includes means for converting the format bidirectionally.

5. An apparatus as set forth in claim 1, wherein the means for converting the format of the control signals includes means for converting the format bidirectionally.

6. An apparatus as set forth in claim 1, wherein the means for converting the format of the data includes at least one means for mapping the data from the format of one device to the format of another device.

7. An apparatus as set forth in claim 6, wherein the data of at least two devices are time-division multiplexed into a plurality of timeslots and the means for mapping includes means for transferring the data from the timeslots of the format of one device to the timeslots of the format of another device.

8. An apparatus as set forth in claim 6, wherein the means for mapping includes at least one means for buffering data.

9. An apparatus as set forth in claim 1, wherein the means for converting the format of the control signals includes state machine means, responsive to control signals in the format of one device, for generating corresponding control signals in the format of another device.

10. An apparatus as set forth in claim 9, wherein the means for converting the format of the control signals further includes at least one server means for conveying control signals to the state machine means.

11. An apparatus as set forth in claim 10, wherein the means for converting the format of the control signals further includes at least one buffer means for buffering control signals passing between the server means and the state machine means.

12. An apparatus as set forth in claim 11, wherein the buffer means includes at least one dual port memory means.

13. An apparatus as set forth in claim 1, wherein the means for converting the format of the control signals includes look-up table means, responsive to control signals in the format of one device, for generating corresponding control signals in the format of another device.

14. An apparatus as set forth in claim 13, wherein the means for converting the format of the control signals further includes at least one server means for conveying control signals to the look-up table means.

15. An apparatus set forth in claim 14, wherein the means for converting the format of the control signals further includes at least one buffer means for buffering control signals passing between the server means and the state machine means.

16. An apparatus set forth in claim 15, wherein the buffer means includes at least one dual port memory means.

17. An apparatus as set forth in claim 1, further including interfacing means for interfacing the apparatus with at least one communications device, wherein the interfacing means includes means for interfacing with at least one serial data highway, at least one serial HDLC link, and timing and synchronization signal lines.

18. An apparatus as set forth in claim 1, further including interfacing means for interfacing the apparatus with at least one communications device, wherein the interfacing means includes means for interfacing with a parallel-format, time-division multiplexed bus containing data and control signals, and lines for timing, synchronization, and card enabling.

19. An apparatus as set forth in claim 18, wherein the bus carries the data and control signals in frames of 576 timeslots.

20. An apparatus as set forth in claim 1, wherein one of the communications devices is a switch and another of the communications devices is subscriber equipment.

21. An apparatus as set forth in claim 1, wherein at least one of the communications devices provides data on at least one serial data highway and control signals on at least one serial HDLC link.

22. An apparatus as set forth in claim 1, wherein at least one of the communications devices provides data and control signals on a parallel-format, time-division multiplexed bus and accepts timing, synchronization, and card enabling signals.

23. An apparatus as set forth in claim 1, wherein the data from at least one device is provided on at least one time-division multiplexed serial highway.

24. An apparatus as set forth in claim 1, wherein the data from at least one device is provided on a parallel-format, time-division multiplexed bus.

25. An apparatus as set forth in claim 24, wherein the bus carries the data within frames of 576 timeslots.

26. An apparatus as set forth in claim 1, wherein the control signals from at least one device are provided on at least one serial HDLC link.

27. An apparatus as set forth in claim 1, wherein the control signals from at least one device are provided on a parallel-format, time-division multiplexed bus.

28. An apparatus as set forth in claim 27, wherein the bus carries control signals within frames of 576 timeslots.

29. An apparatus for interfacing at least two communications devices, at least one device accepting data on at least one serial data highway and control signals on at least one serial HDLC link, comprising:

means for accepting data; and

means for converting the format of the data to the format of that one device in real time.

30. An apparatus for interfacing at least two communications devices, at least one device accepting data on a parallel-format, time-division multiplexed bus, where the bus carries data and control signals time-multiplexed on the bus, comprising:

means for accepting data; and

means for converting the format of the data to the format of that one device in real time.

31. An apparatus for interfacing at least two communications devices, at least one device accepting control signals on at least one serial HDLC link and data on at least one serial data highway, comprising:

means for accepting control signals; and

means for converting the format of the control signals to the format of that one device in real time.

32. An apparatus for interfacing at least two communications devices, at least one device accepting control signals on a parallel-format, time-division multiplexed bus, where the bus carries data and control signals time-multiplexed on the bus, comprising:

means for accepting control signals; and

means for converting the format of the control signals to the format of that one device in real time.

33. An apparatus, comprising:

switch means having formats for data and control signals;

subscriber equipment means having formats for data and control signals;

means for interfacing the switch means and the subscriber equipment means.

34. An apparatus as set forth in claim 33, wherein the means for interfacing includes:

means for converting the format of the data from the format of one device to the format of another device; and

means for converting the format of the control signals from the format of one device to the format of another device.

35. An apparatus as set forth in claim 34, wherein the means for converting the format of the data includes means for converting the format in real time and the means for converting the format of the control signals includes means for converting the format in real time.

36. An apparatus as set forth in claim 34, wherein the means for converting the format of the data includes means for converting the format bidirectionally and the means for converting the format of the control signals includes means for converting the format bidirectionally.

37. A method of interfacing at least two communications devices, each device accepting data and control signals, and each device having formats for data and control signals, comprising the steps of:

converting the format of the data from the format of one device to the format of another device; and

converting the format of the control signals from the format of one device to the format of another device.

38. A method as set forth in claim 37, wherein the step of converting the format of the data is performed in real time.

39. A method as set forth in claim 37, wherein the step of converting the format of the control signals is performed in real time.

40. A method as set forth in claim 37, wherein the step of converting the format of the data is performed bidirectionally.

41. A method as set forth in claim 37, wherein the step of converting the format of the control signals is performed bidirectionally.

42. A method as set forth in claim 37, wherein the step of converting the format of the data includes the step of mapping the data from the format of one device to the format of another device.

43. A method as set forth in claim 42, wherein the data of at least two devices are time-division multiplexed into a plurality of timeslots and wherein the step of mapping includes the step of transferring the data from the timeslots of the format of one device to the timeslots of the format of another device.

44. A method as set forth in claim 37, wherein the step of converting the format of the control signals includes the step of, in response to control signals in the format of one device, generating corresponding control signals in the format of another device.

45. A method as set forth in claim 37, where at least one device provides data on at least one serial data highway and control signals on at least one serial HDLC link, and further provides timing and synchronization signals.

46. A method as set forth in claim 37, where at least one device provides data and control signals on a parallel-format, time-division multiplexed bus, and accepts timing, synchronization, and card enabling signals

47. A method as set forth in claim 37, wherein the data from at least one device is provided on at least one time-division multiplexed serial highway.

48. A method as set forth in claim 37, wherein the data from at least one device is provided on a parallel-format, time-division multiplexed bus.

49. A method as set forth in claim 48, wherein the bus carries the data within frames of 576 timeslots.

50. A method as set forth in claim 37, wherein the control signals from at least one device are provided on at least one serial HDLC link.

51. A method as set forth in claim 37, wherein the control signals from at least one device are provided on a parallel-format, time-division multiplexed bus.

52. A method as set forth in claim 51, wherein the bus carries control signals within frames of 576 timeslots.

53. A method of interfacing at least two communications devices, at least one device accepting data on at least one serial data highway and control signals on at least one serial HDLC link, comprising the steps of:

accepting data; and

converting the format of the data to the format of that one device in real time.

54. A method of interfacing at least two communications devices, at least one device accepting data on a parallel-format, time-division multiplexed bus, where the bus carries data and control signals time-multiplexed on the bus, comprising the steps of:

accepting data; and

converting the format of the data to the format of that one device in real time.

55. A method of interfacing at least two communications devices, at least one device accepting control signals on at least one serial HDLC link and data on at least one serial data highway, comprising the steps of:

accepting control signals; and

converting the format of the control signals to the format of that one device in real time.

56. A method of interfacing at least two communications devices, at least one device accepting control signals on a parallel-format, time-division multiplexed bus, where the bus carries data and control signals time-multiplexed on the bus, comprising the steps of:

accepting control signals; and

converting the format of the control signals to the format of that one device in real time.

FIG. 1

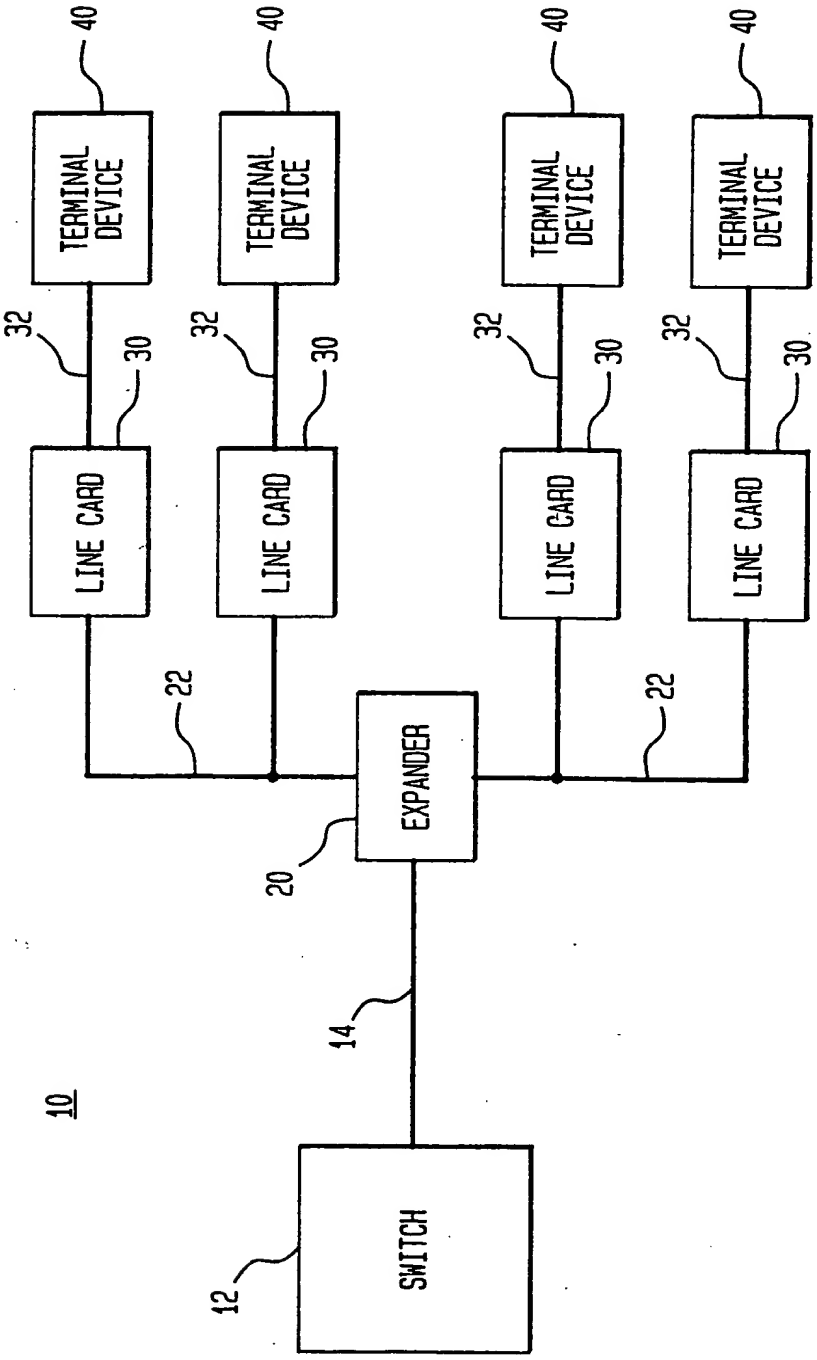
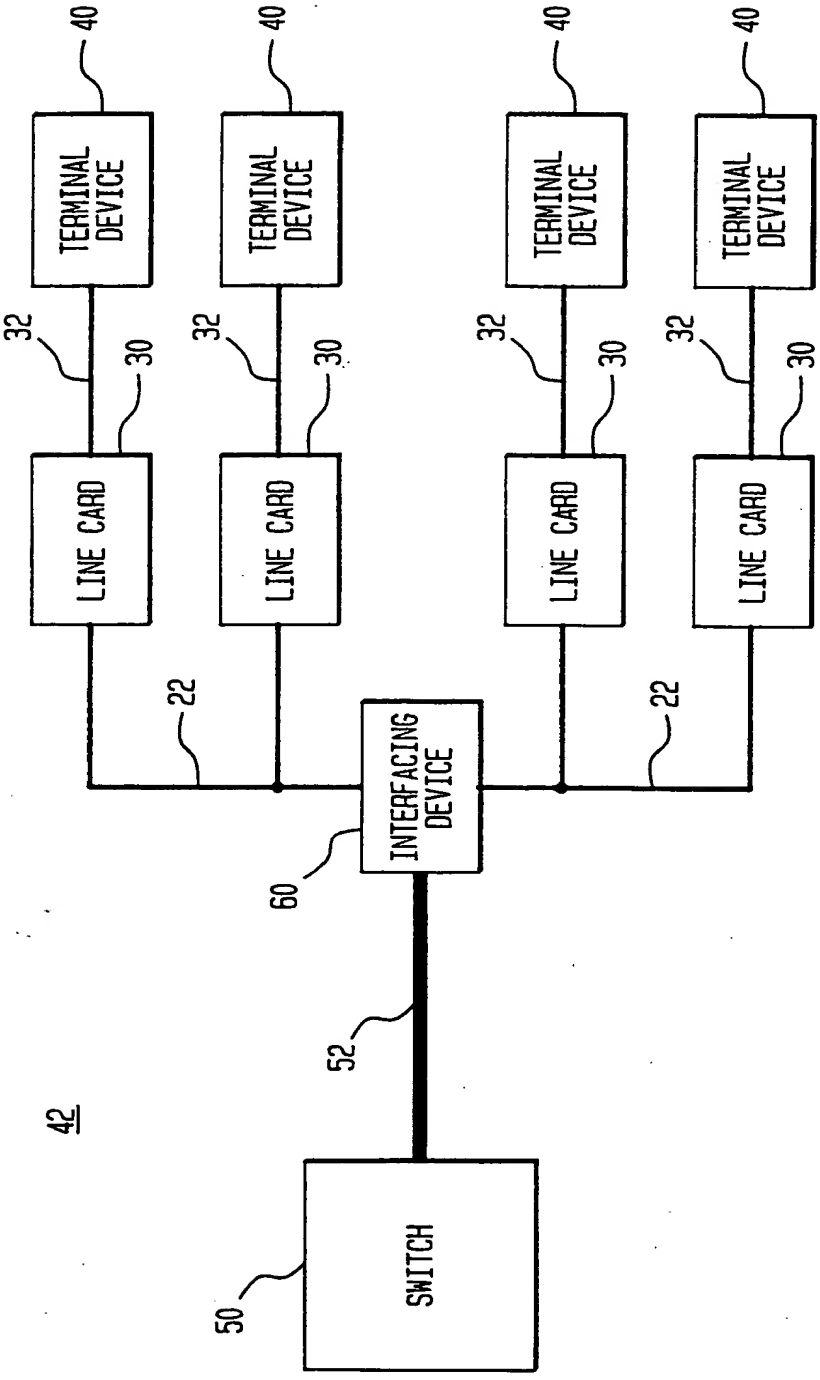

10
SWITCH
12
14
EXPANDER
20
22
22
LINE CARD
LINE CARD
LINE CARD
LINE CARD
30
30
30
30
32
32
32
32
TERMINAL DEVICE
TERMINAL DEVICE
TERMINAL DEVICE
TERMINAL DEVICE
40
40
40
40

FIG. 2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LINE CARD
30
32
22
INTERFACING DEVICE
60
52
SWITCH
50
42

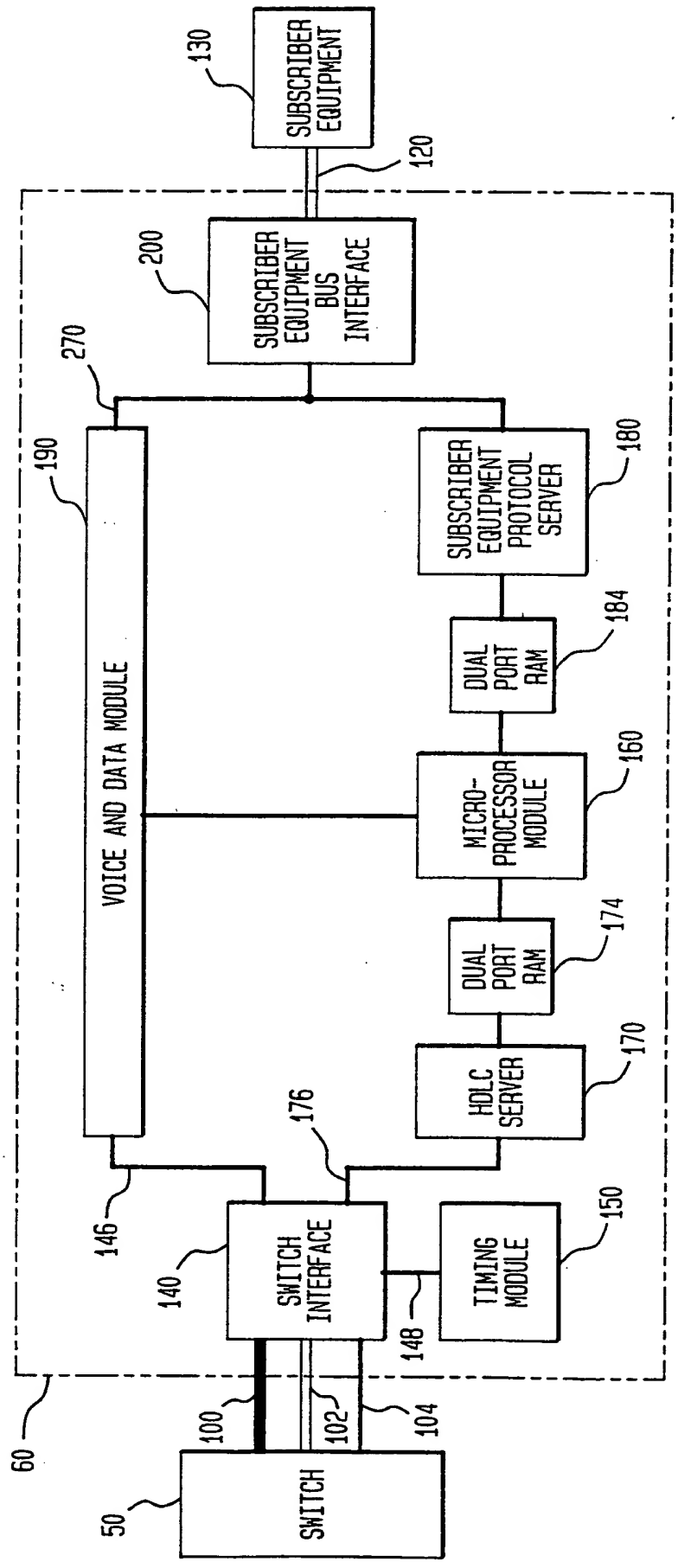

SUBSCRIBER EQUIPMENT
130
120
SUBSCRIBER EQUIPMENT BUS INTERFACE
200
270
190
VOICE AND DATA MODULE
SUBSCRIBER EQUIPMENT PROTOCOL SERVER
180
DUAL PORT RAM
184
MICRO-PROCESSOR MODULE
160
DUAL PORT RAM
174
HDLC SERVER
170
176
146
140
SWITCH INTERFACE
TIMING MODULE
150
148
100
102
104
60
50
SWITCH

FIG. 3

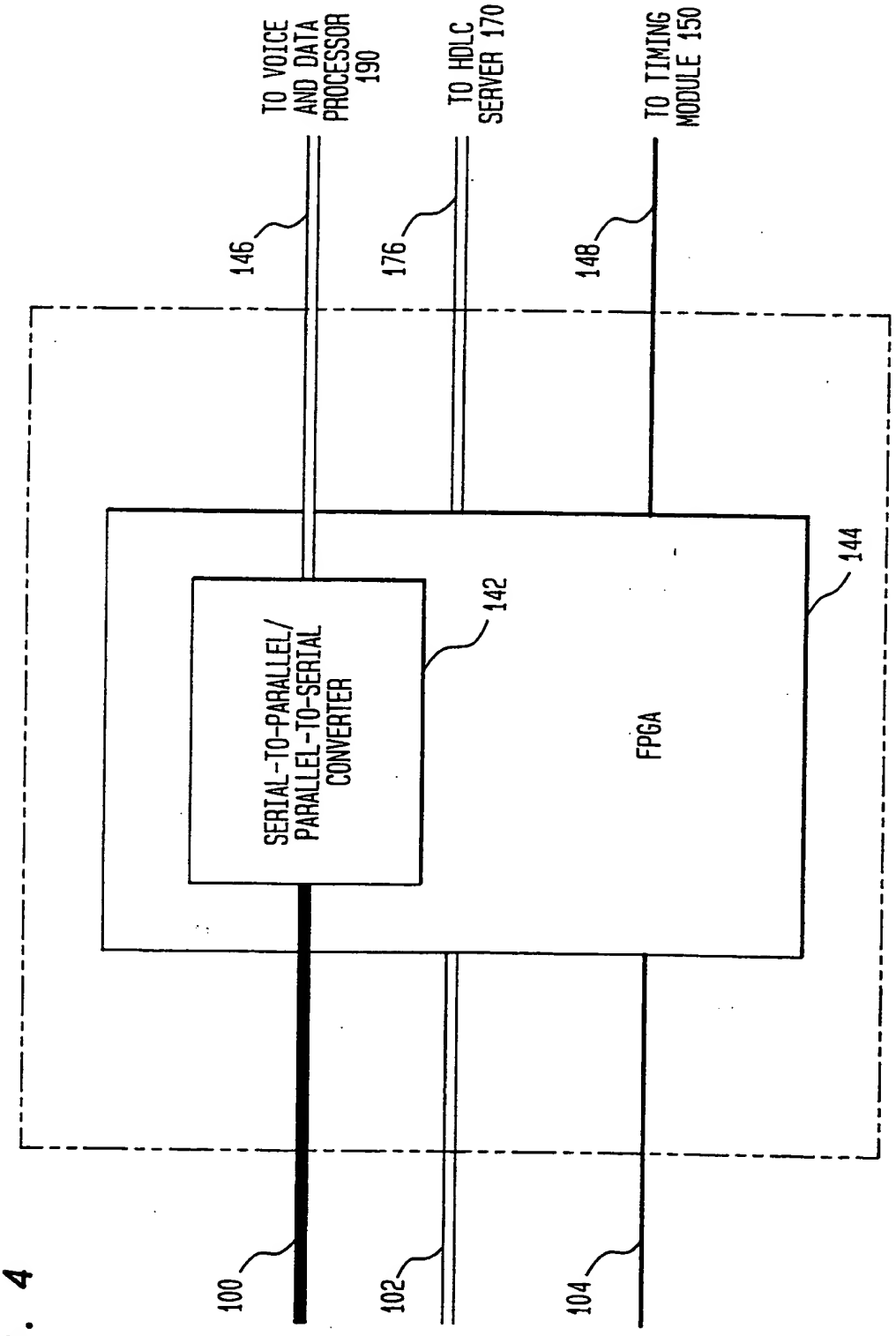

TO VOICE AND DATA PROCESSOR 190
TO HDLC SERVER 170
TO TIMING MODULE 150
146
176
148
SERIAL-TO-PARALLEL/ PARALLEL-TO-SERIAL CONVERTER
142
FPGA
144
140
100
102
104

FIG. 4

FIG. 5

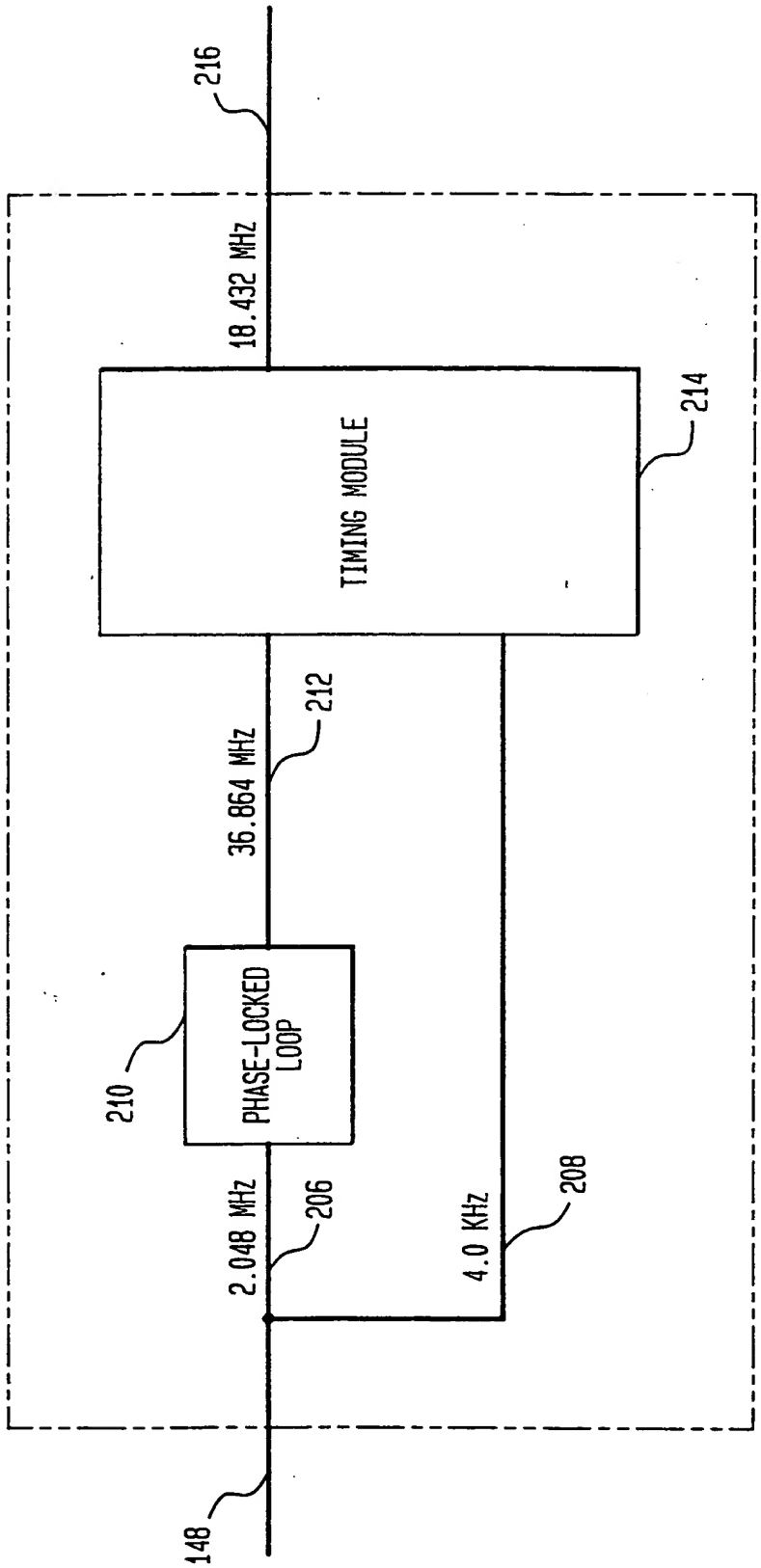

216
18.432 MHz
TIMING MODULE
214
212
36.864 MHz
210
PHASE-LOCKED LOOP
2.048 MHz
206
4.0 KHz
208
148
150

FIG. 6

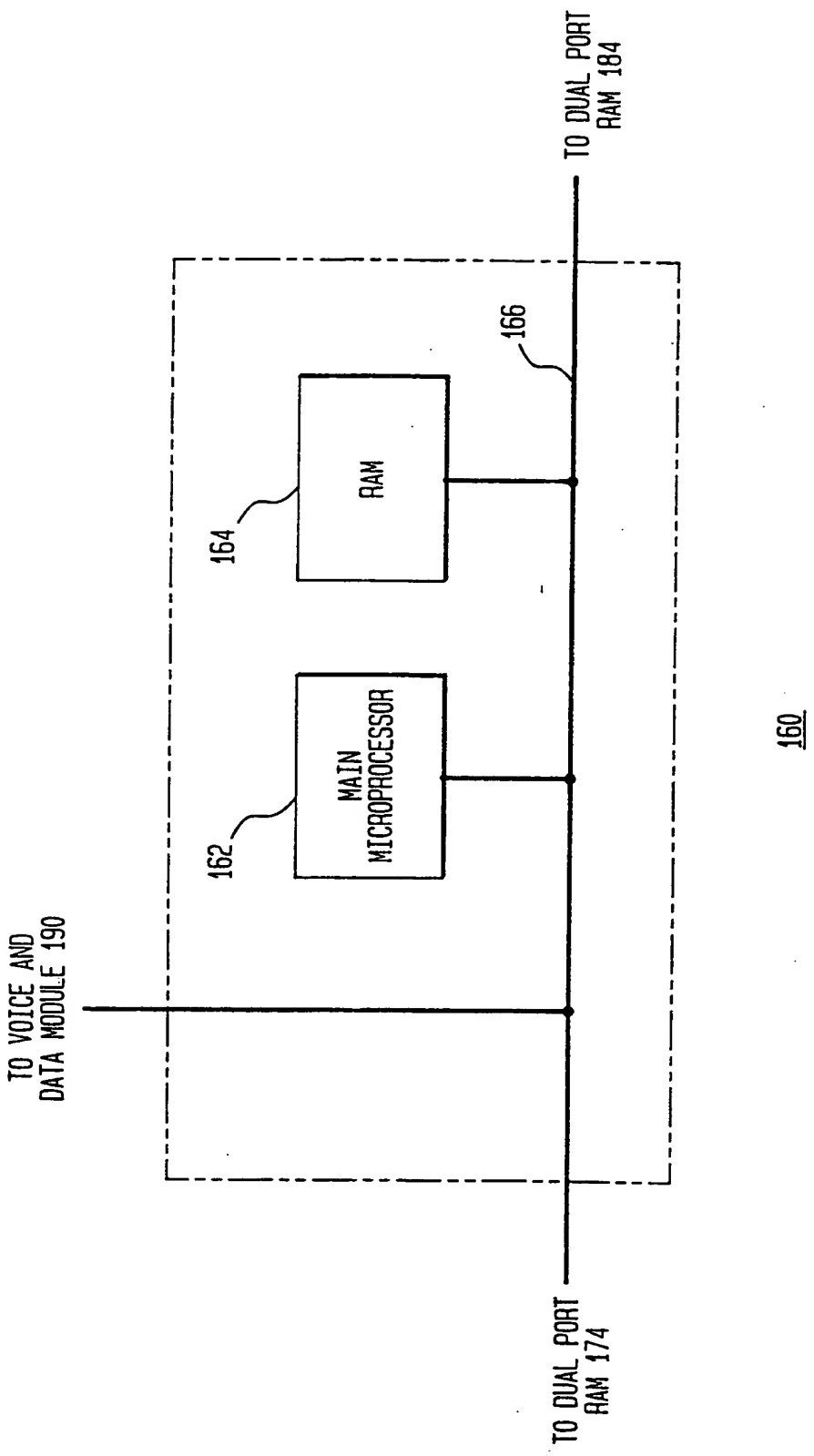

TO DUAL PORT RAM 184
166
RAM
164
MAIN MICROPROCESSOR
162
TO VOICE AND DATA MODULE 190
TO DUAL PORT RAM 174
160

FIG. 7

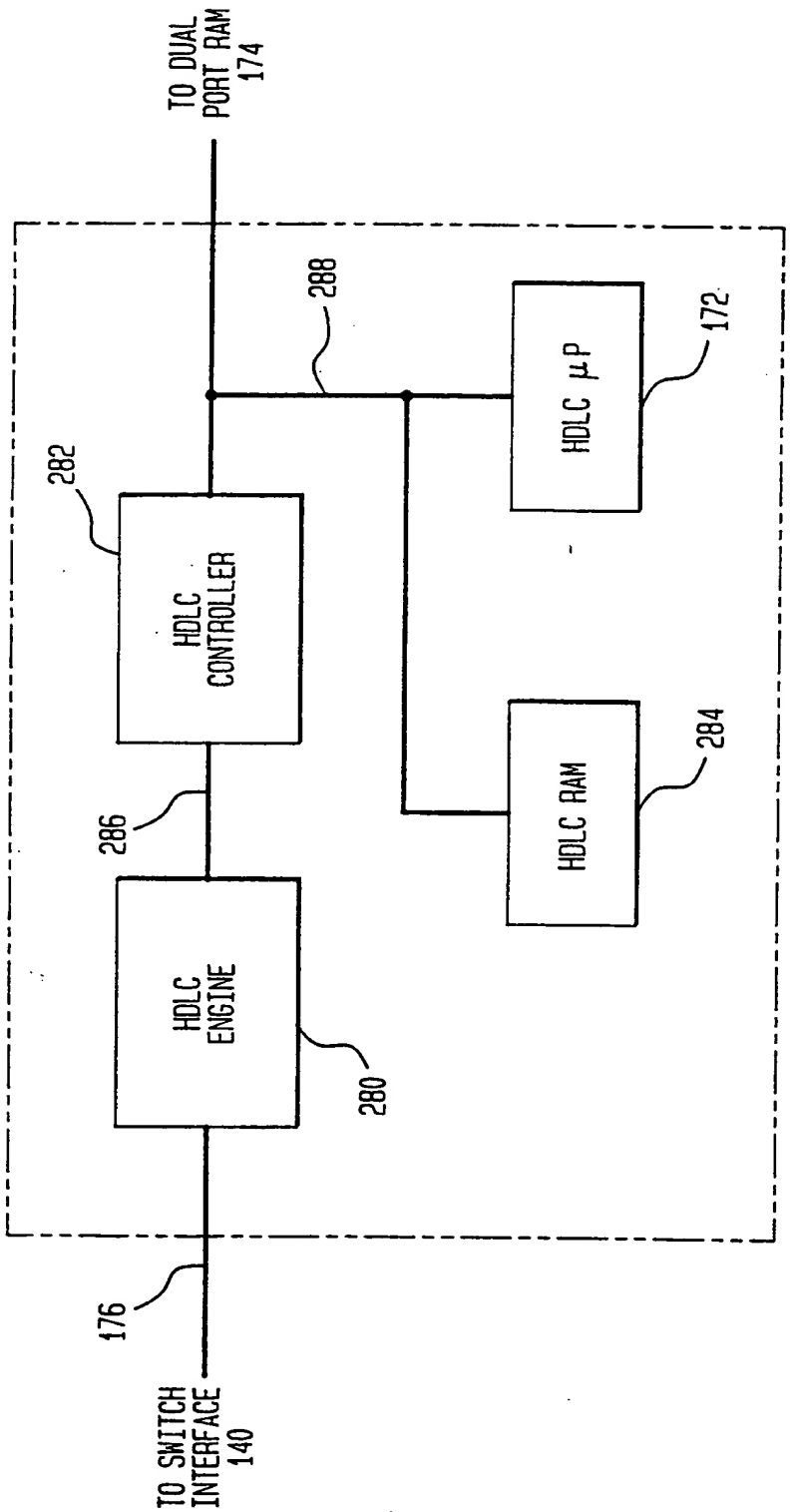

TO DUAL PORT RAM 174
288
HDLC μP
172
282
HDLC CONTROLLER
HDLC RAM
284
286
HDLC ENGINE
280
170
176
TO SWITCH INTERFACE 140

FIG. 8

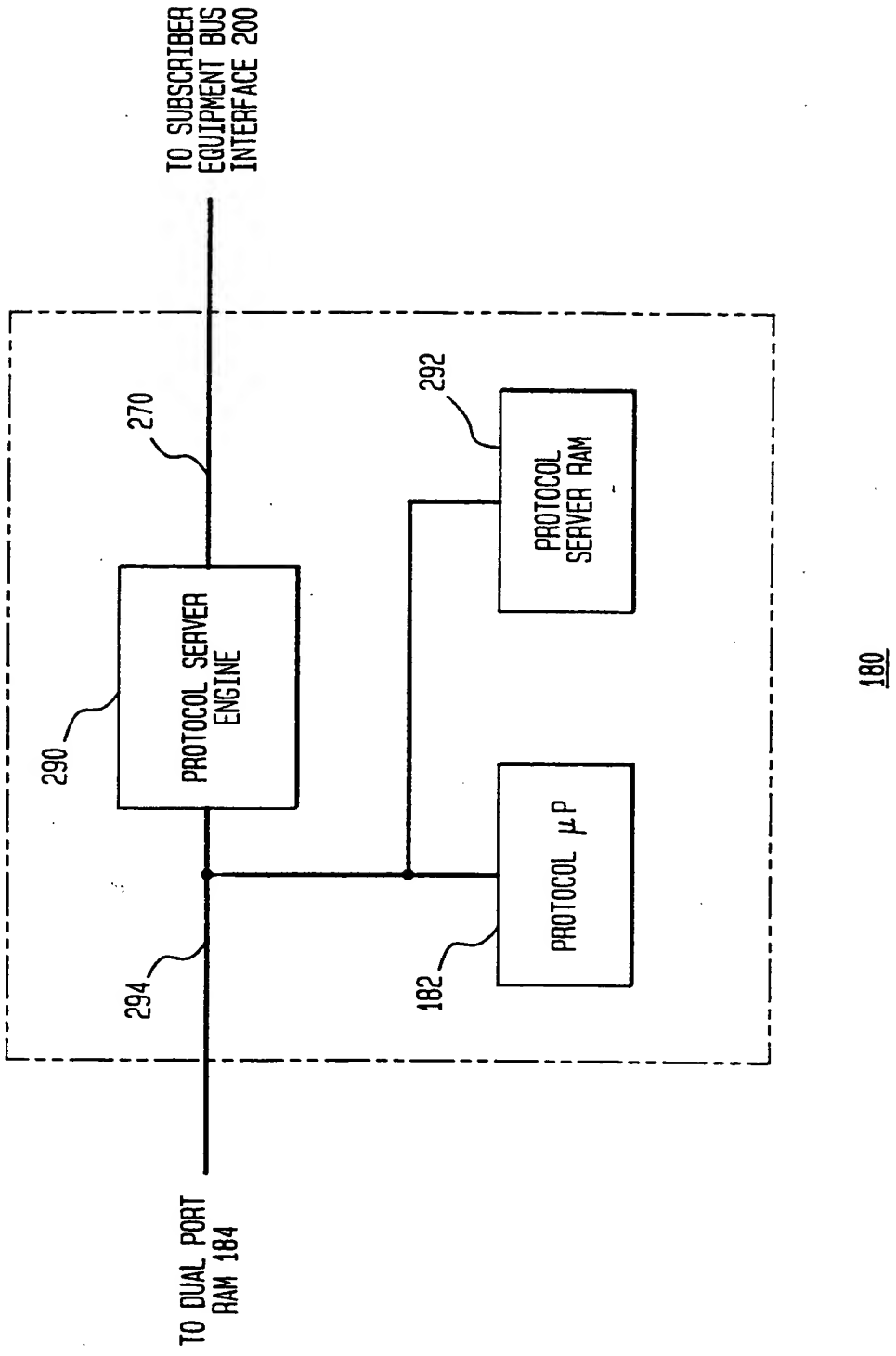

TO SUBSCRIBER EQUIPMENT BUS INTERFACE 200
270
292
PROTOCOL SERVER RAM
290
PROTOCOL SERVER ENGINE
PROTOCOL μP
294
182
TO DUAL PORT RAM 184
180

FIG. 9

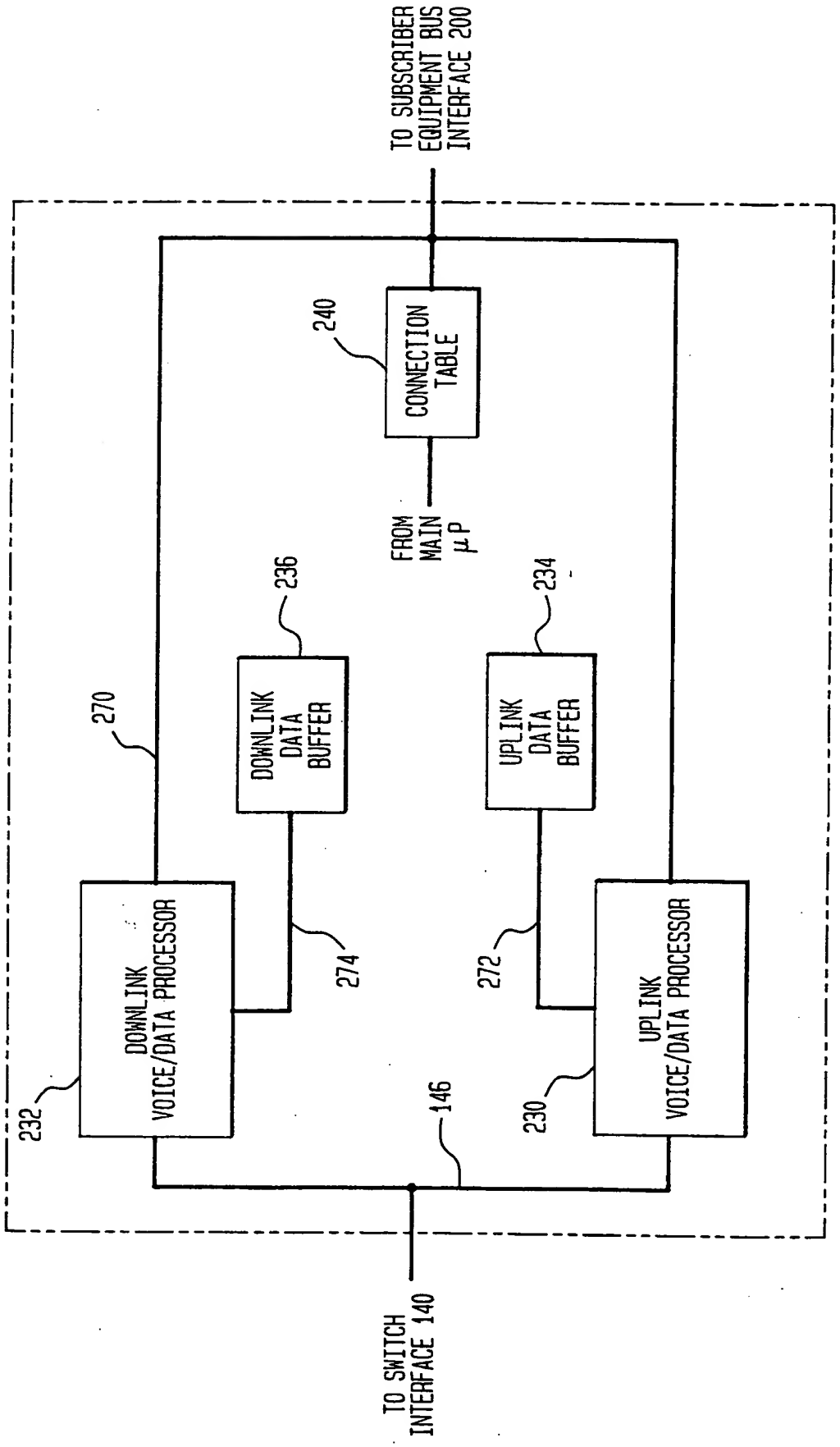

TO SUBSCRIBER EQUIPMENT BUS INTERFACE 200
240
CONNECTION TABLE
FROM MAIN μP
236
DOWNLINK DATA BUFFER
234
UPLINK DATA BUFFER
270
274
272
DOWNLINK VOICE/DATA PROCESSOR
UPLINK VOICE/DATA PROCESSOR
232
230
146
TO SWITCH INTERFACE 140
190

FIG. 10

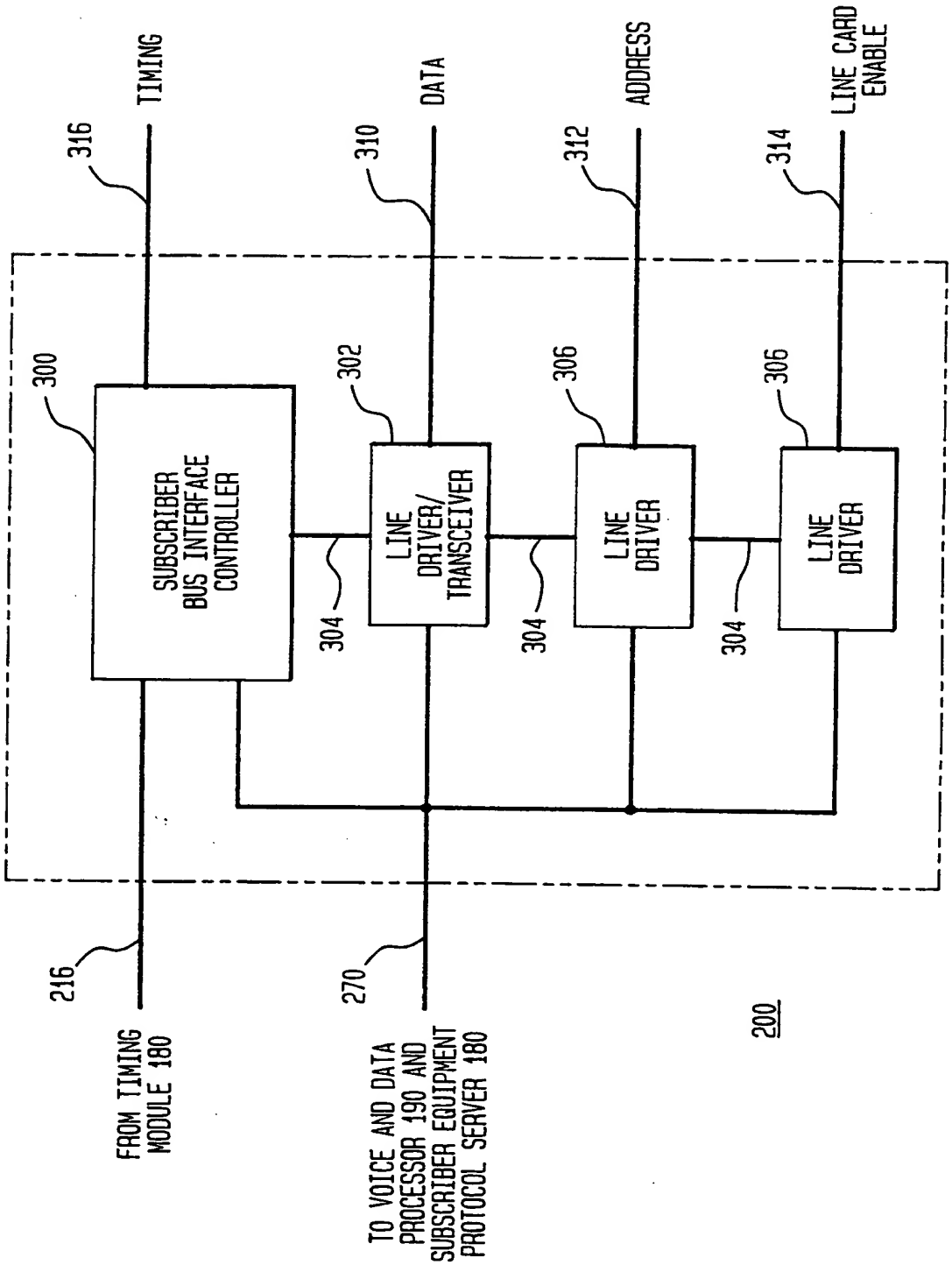

TIMING
DATA
ADDRESS
LINE CARD ENABLE
316
310
312
314
300
302
306
306
SUBSCRIBER BUS INTERFACE CONTROLLER
LINE DRIVER/ TRANSCEIVER
LINE DRIVER
LINE DRIVER
304
304
304
216
270
FROM TIMING MODULE 180
TO VOICE AND DATA PROCESSOR 190 AND SUBSCRIBER EQUIPMENT PROTOCOL SERVER 180
200

FIG. 11

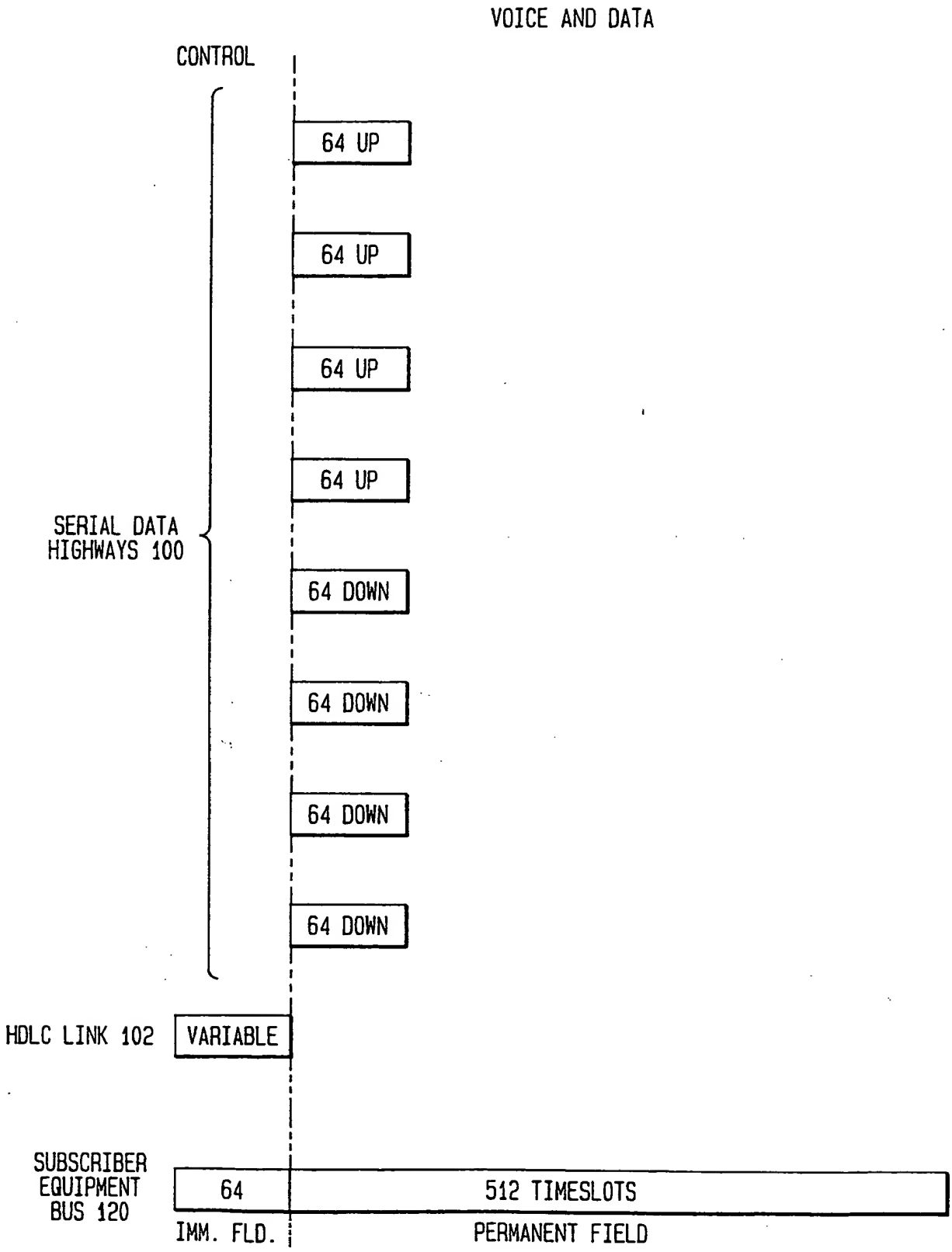
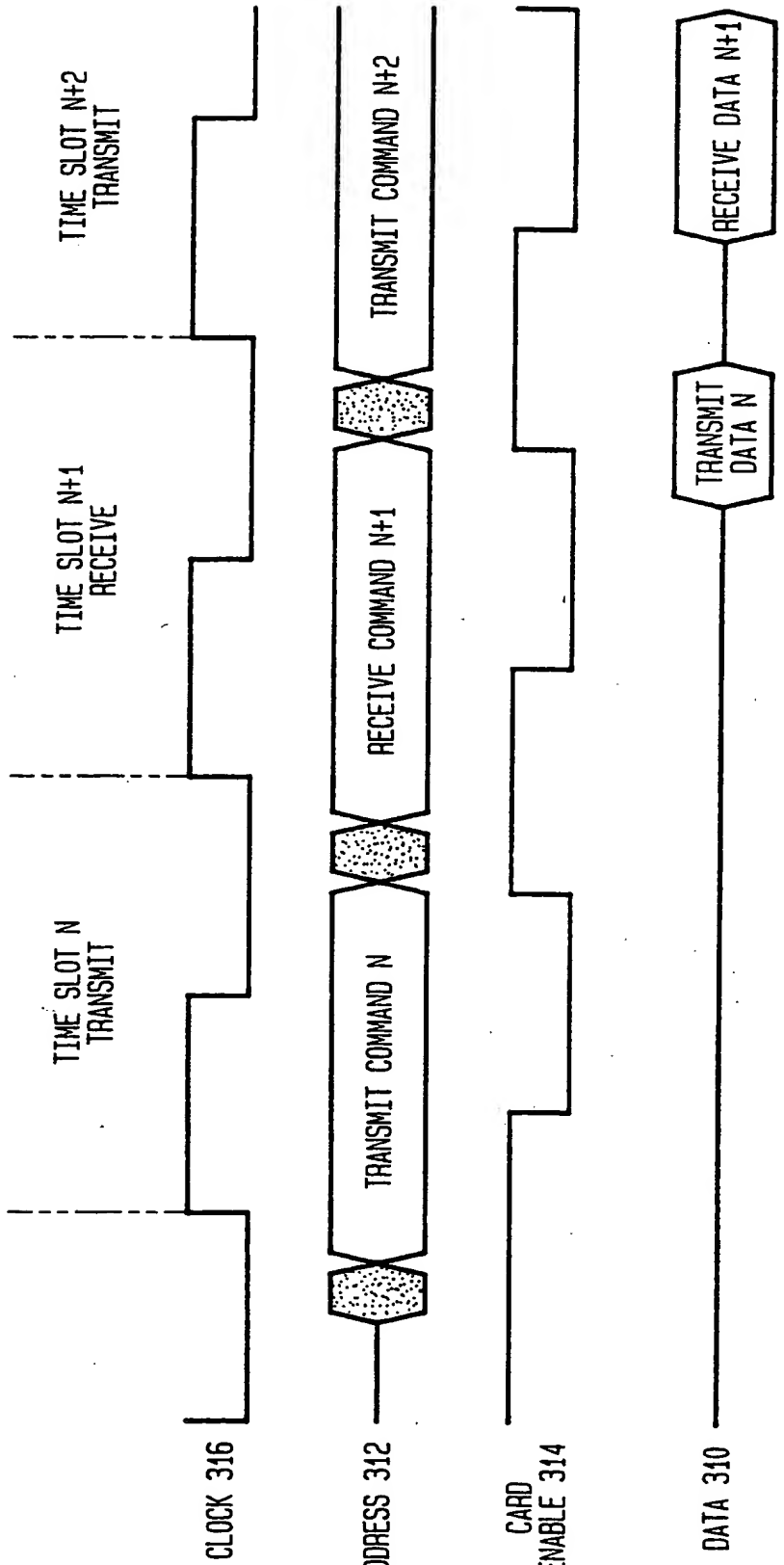

VOICE AND DATA
CONTROL
64 UP
64 UP
64 UP
64 UP
SERIAL DATA HIGHWAYS 100
64 DOWN
64 DOWN
64 DOWN
64 DOWN
HDLC LINK 102
VARIABLE
SUBSCRIBER EQUIPMENT BUS 120
64
512 TIMESLOTS
IMM. FLD.
PERMANENT FIELD

FIG. 12


TIME SLOT N
TRANSMIT
TIME SLOT N+1
RECEIVE
TIME SLOT N+2
TRANSMIT
TRANSMIT COMMAND N
RECEIVE COMMAND N+1
TRANSMIT COMMAND N+2
TRANSMIT DATA N
RECEIVE DATA N+1
CLOCK 316
ADDRESS 312
CARD ENABLE 314
DATA 310

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 94/05554

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 H04L29/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A,4 783 778 (W.W.FINCH ET AL) 8 November 1988 see claim 1 see abstract	1-5, 29-33, 37-41, 53-56
A	EP,A,0 429 054 (DIGITAL EQUIPMENT CORP.) 29 May 1991 see claims 1,11	1-56
A	EP,A,0 193 139 (INTERNATIONAL STANDARD ELECTRIC CORP.) 3 September 1986 see page 6, line 6 - page 9, line 25	1-56

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 September 1994	07. 10. 94

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Canosa Areste, C

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US 94/05554

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A-4783778	08-11-88	NONE		
EP-A-0429054	29-05-91	US-A-	5175817	29-12-92
		AU-B-	627375	20-08-92
		AU-A-	6572890	18-07-91
		CA-A-	2029259	21-05-91
		JP-A-	3239046	24-10-91
EP-A-0193139	03-09-86	US-A-	4677611	30-06-87
		AU-A-	5344286	28-08-86
		JP-A-	61196645	30-08-86